

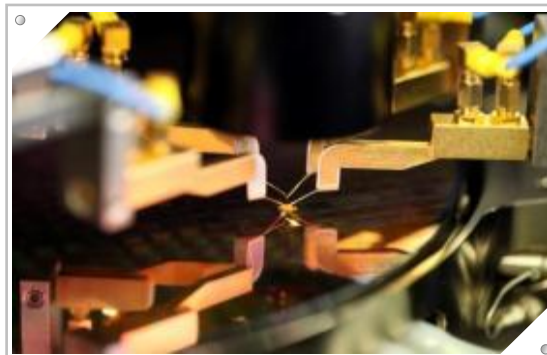
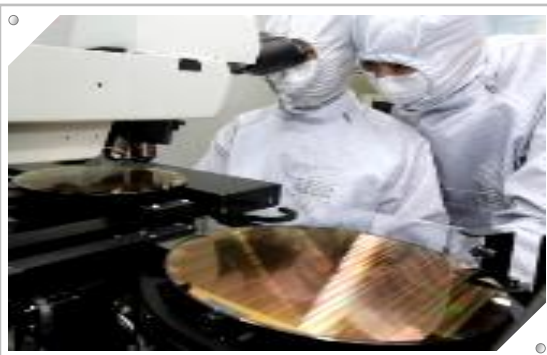
DB HiTek

World Leader In Specialty Foundry

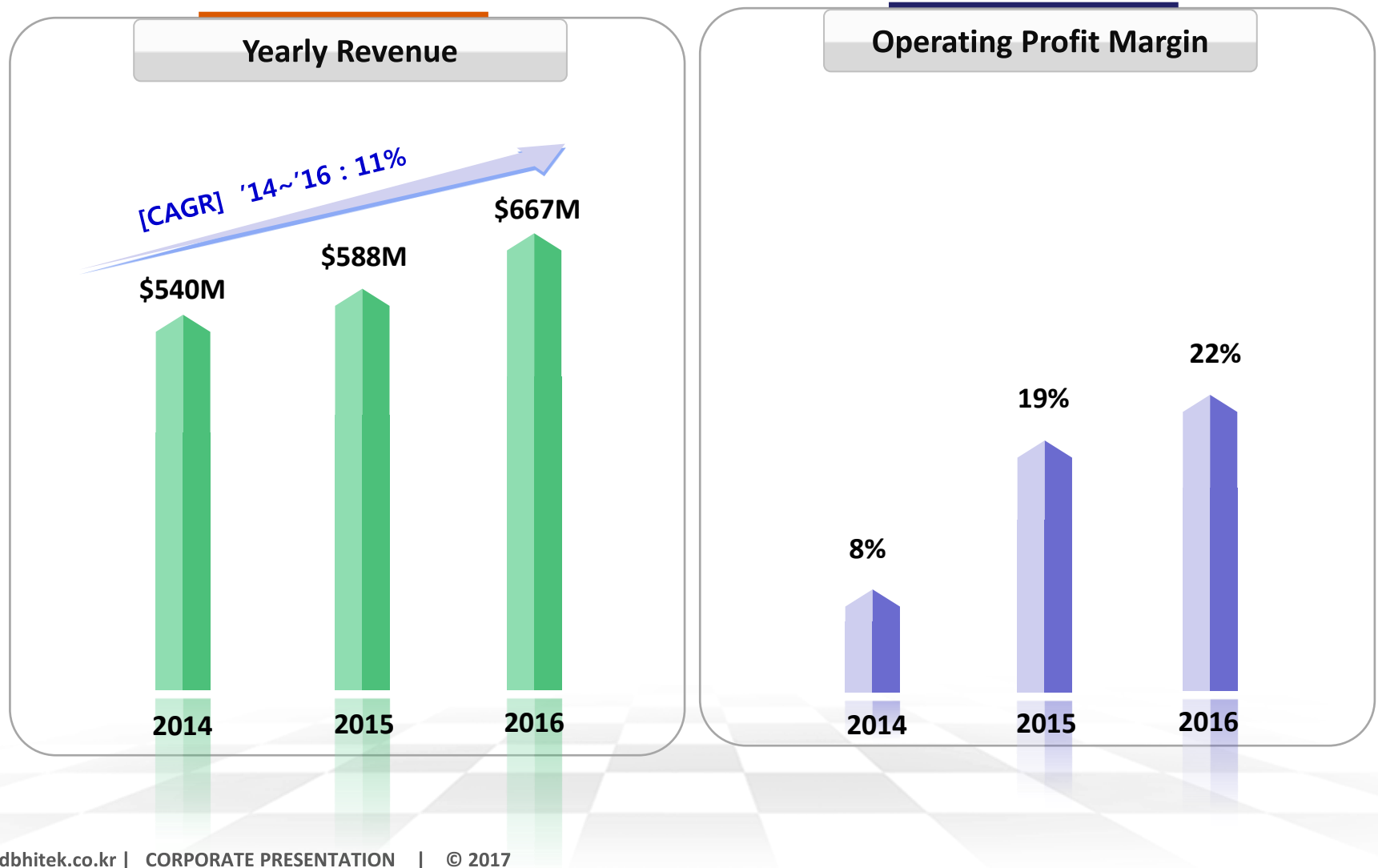


Company Overview

● Established	1997
● Revenue(2016)	US\$667M
● Asset(2016)	US\$817M
● Number of Employees	2,100 (Jan. 2017)
● Business Areas	System IC
● Technology	90nm~0.35um
● Capacity	116,000wfs/month (200mm)



- Consecutive revenue and margin growth from 2013



History



Management Team



**Changsik Choi,
CEO**



**KS Cho,
Senior VP,
Foundry Business**



**CH Choi
VP,
Brand Business**



**YJ Lee,
Senior VP,
Technology Development**



**YG Choi,
VP,
Manufacturing**



**WS Kim,
VP,
QRA**



**JH Kang,
VP,
Product Engineering**



**GH Koo
CFO, Senior VP,
Strategy Planning**



Fab1 (Bucheon)



Fab2 (Sangwoo)

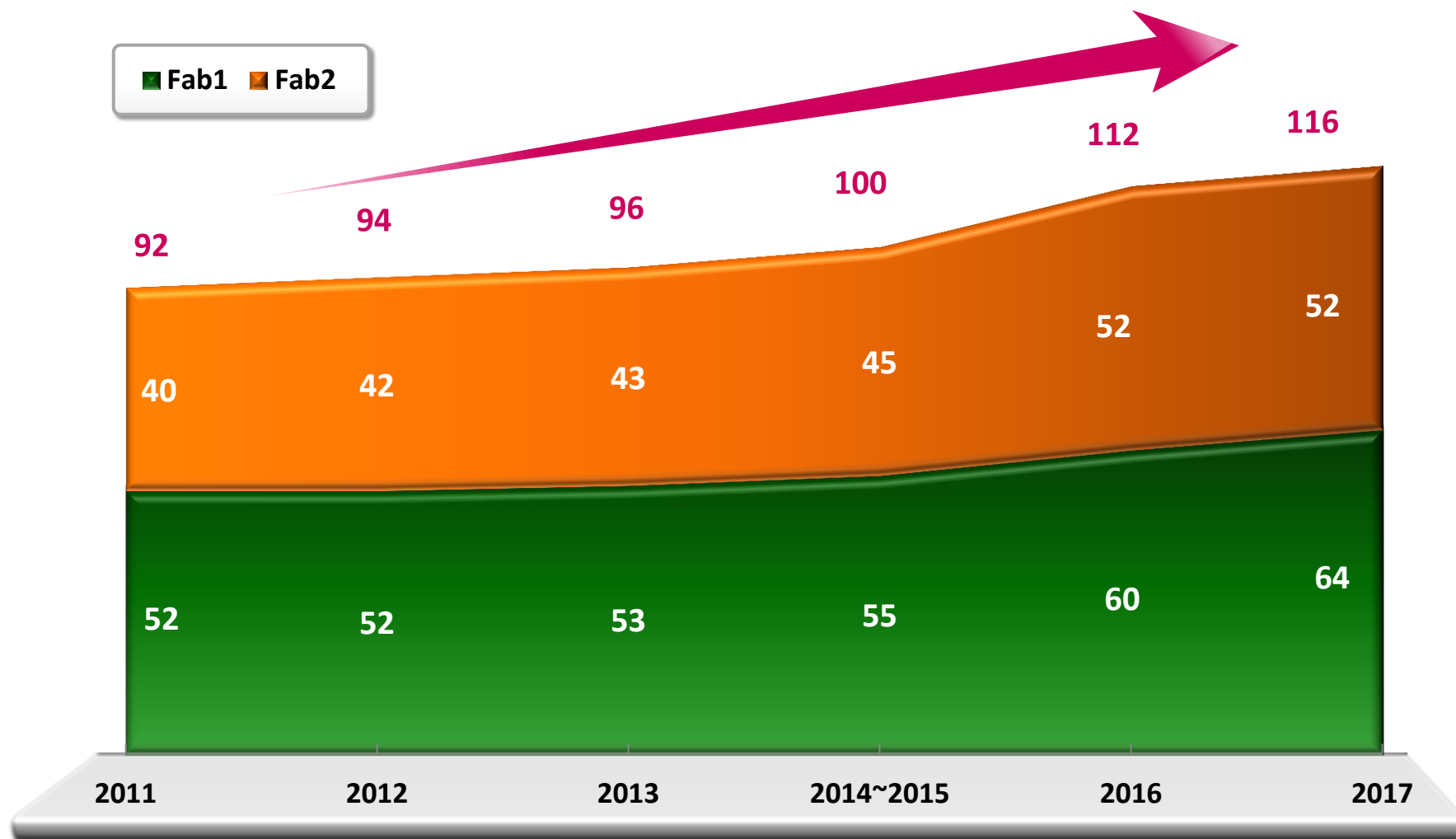


Capacity	64,000wfs/month	52,000wfs/month
Technology	0.35, 0.25, 0.18, 0.15um	0.18, 0.13, 0.11, 0.09um
Key Process	Analog/ Power, Mixed-Signal, High Voltage CMOS, SJ MOSFET	Analog/ Power, Mixed-Signal, CIS, eFlash, High Voltage CMOS, MEMS
Wafer Size	200mm(8 inch)	200mm(8 inch)
Location	Bucheon, Gyunggi-do	Eumsung, Chungcheongbuk-do

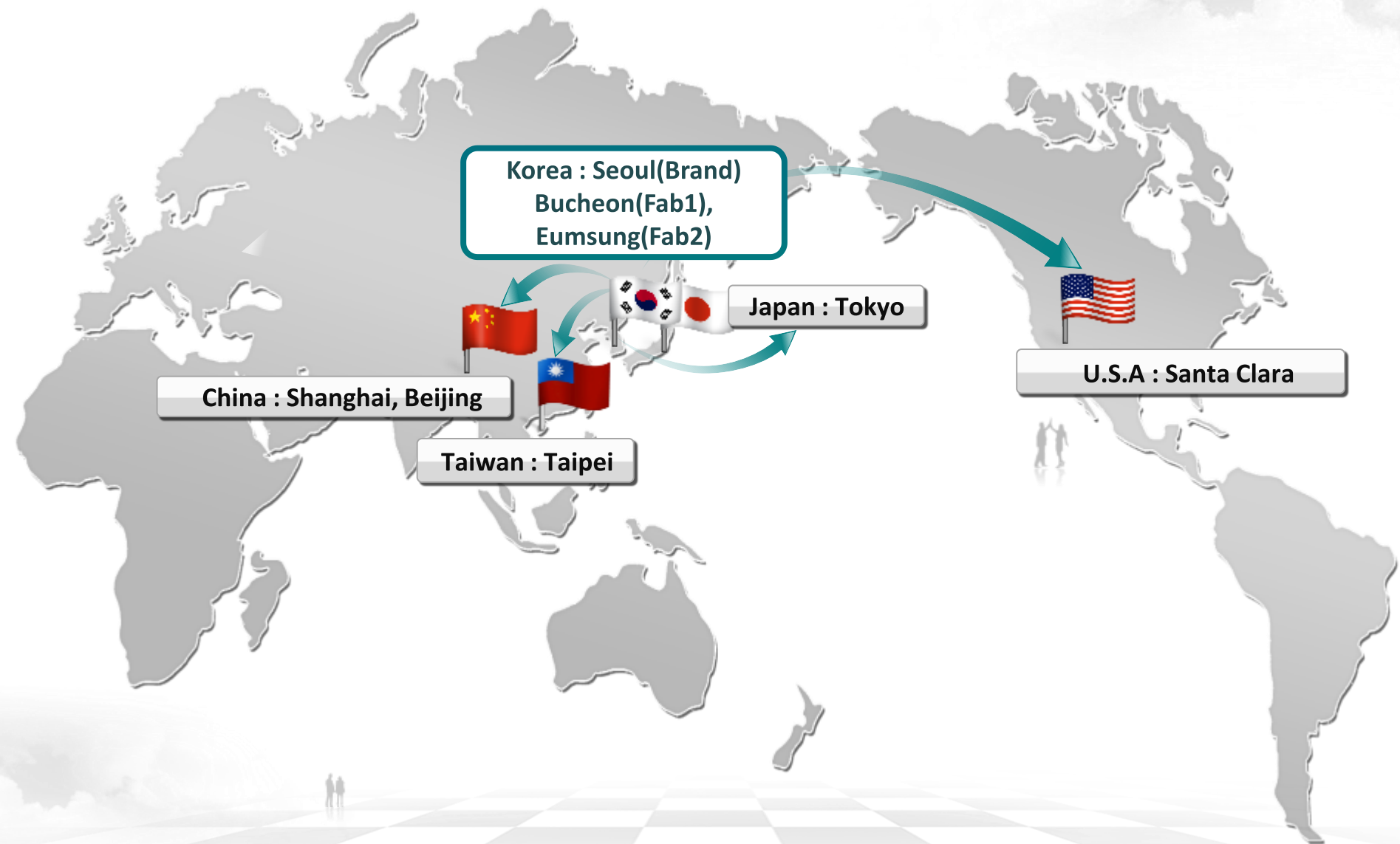
Capacity

● Continue to expand the capacity

(Unit: Kwfs/month)



Global Networks



Certifications

Quality Certification



ISO 9001



ISO/TS 16949

ESH Certification



ISO 14001

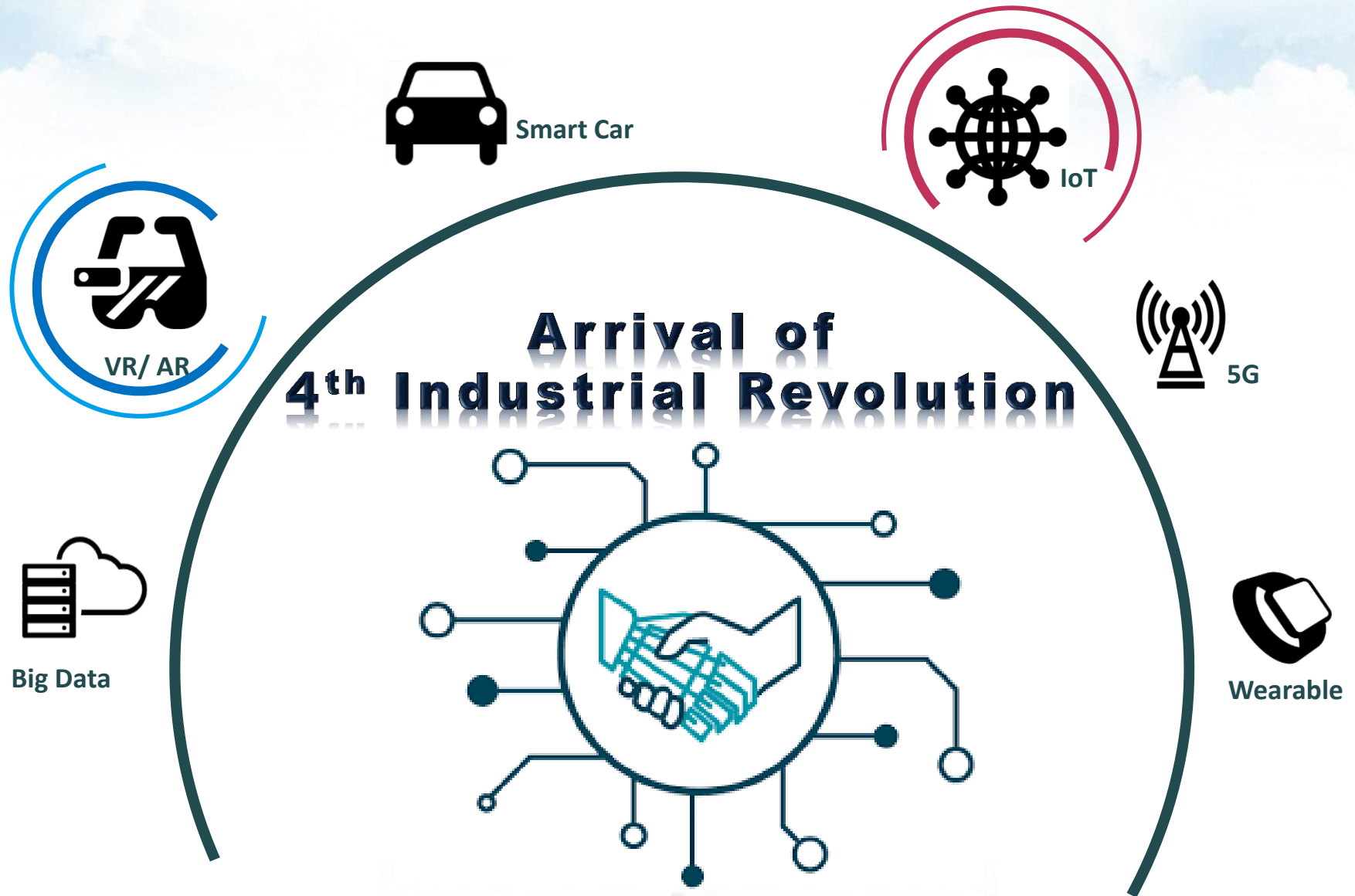


OHSAS 18001

Security Certification

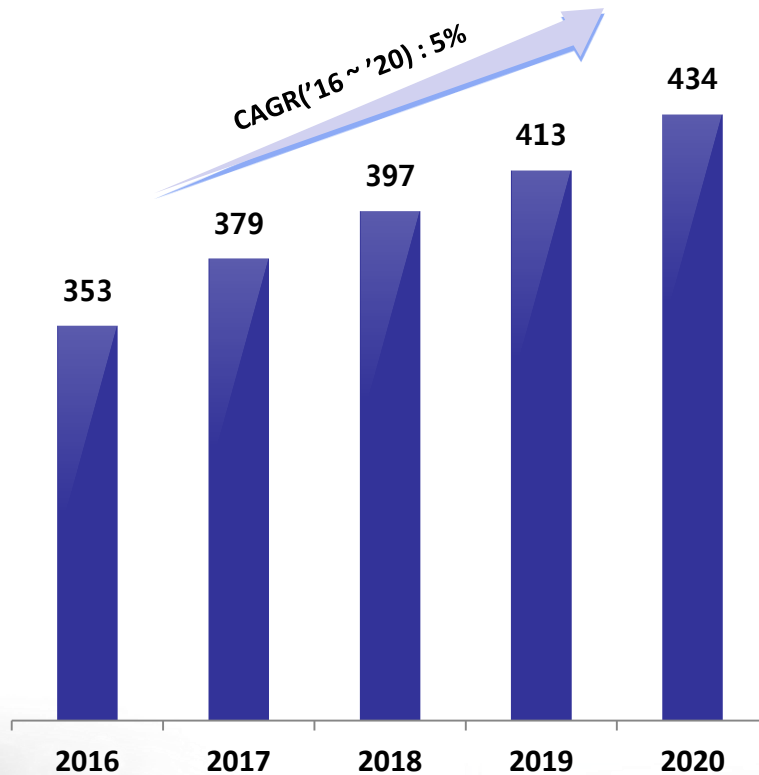


ISO 27001



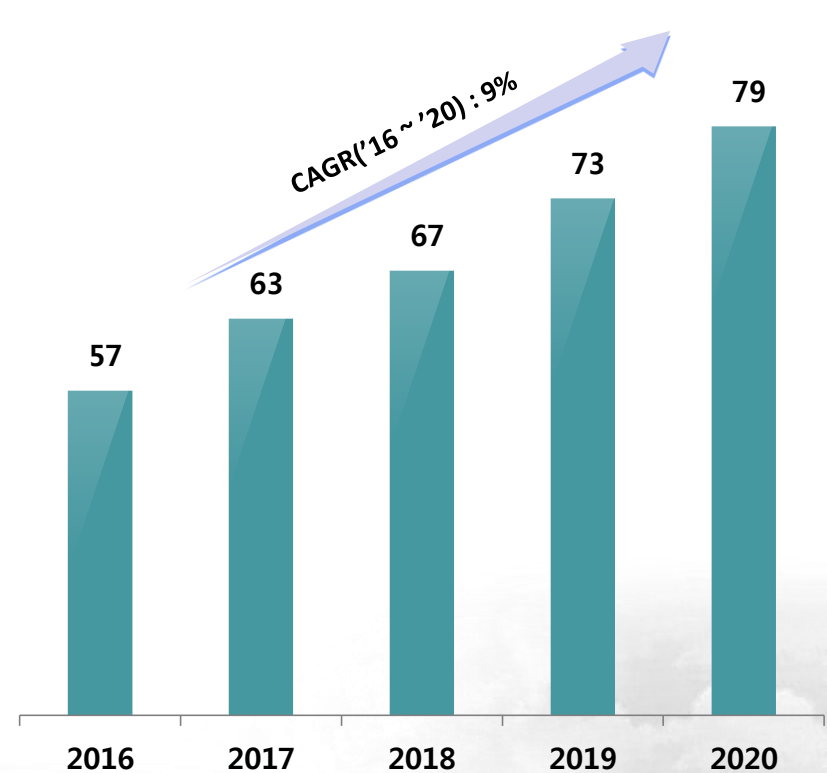
Global Semiconductor

(Unit: \$B)



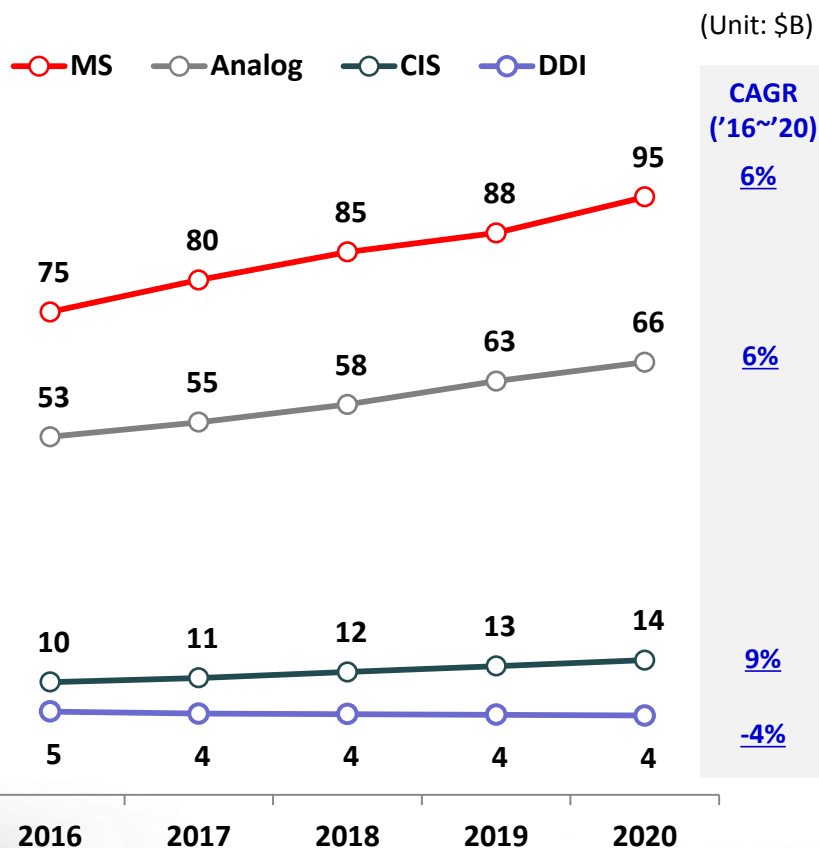
Foundry

(Unit: \$B)



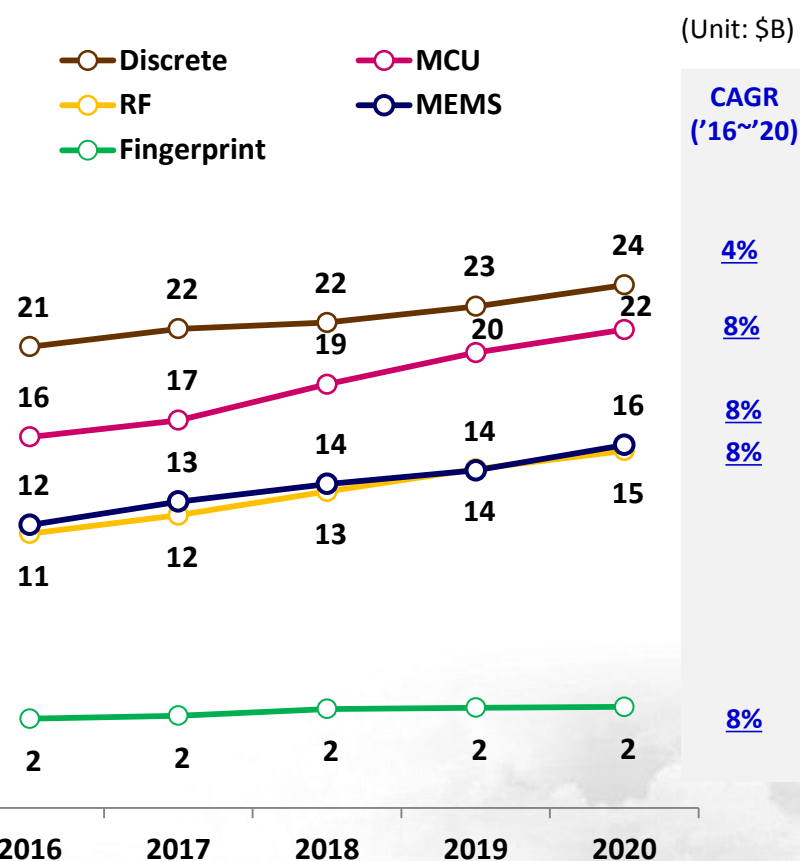
(Source: IHS '16.4Q)

Target Products (As- Is)



※ DDI CAGR('16 ~ '20) : UHD 3%, OLED 16%

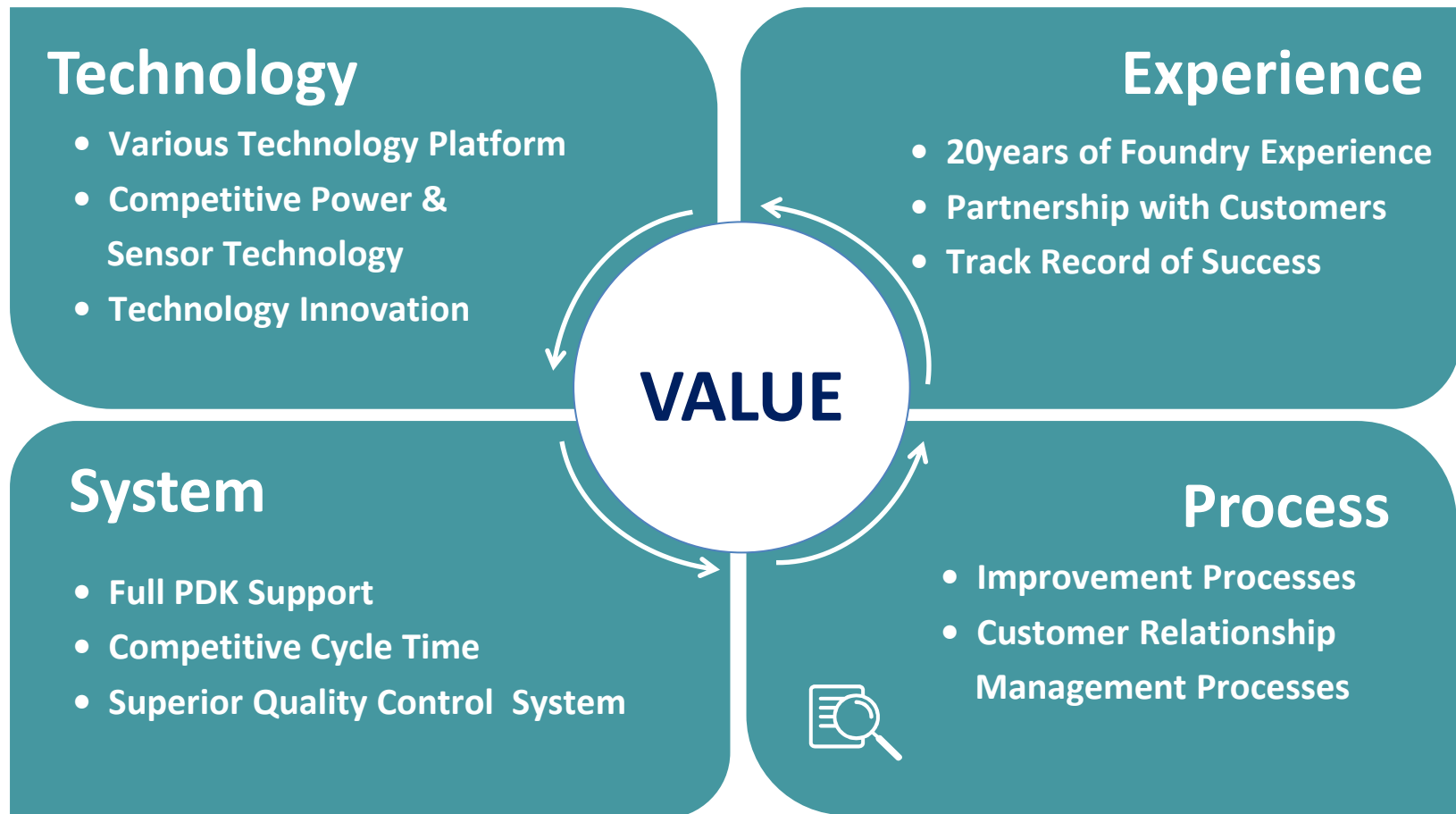
Target Products (New)



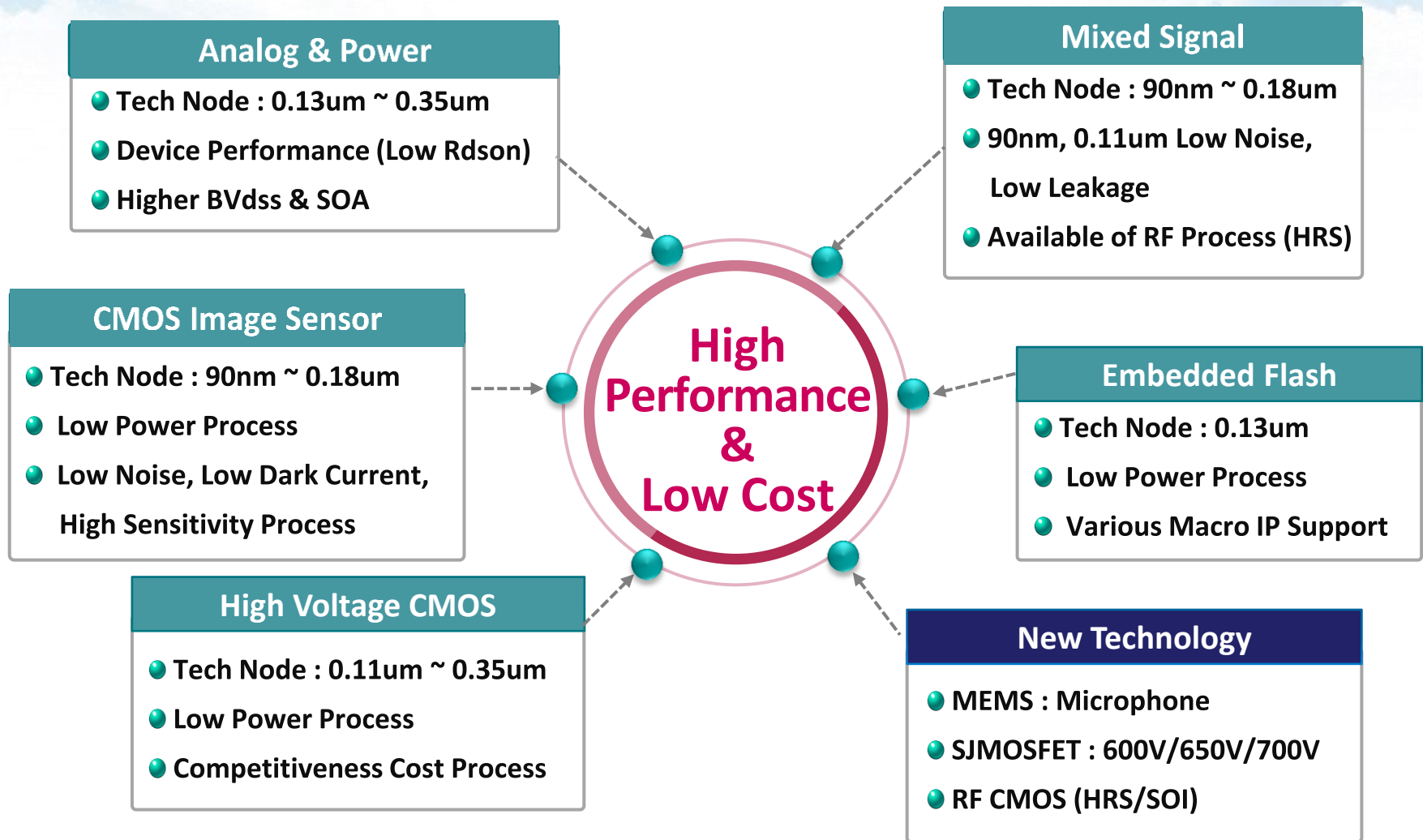
(Source: IHS '16.4Q, Gartner '16.4Q, Credit Suisse '16.1, Yuanta Investment Consulting '16.12, DBH Estimation)

Foundry Value Proposition

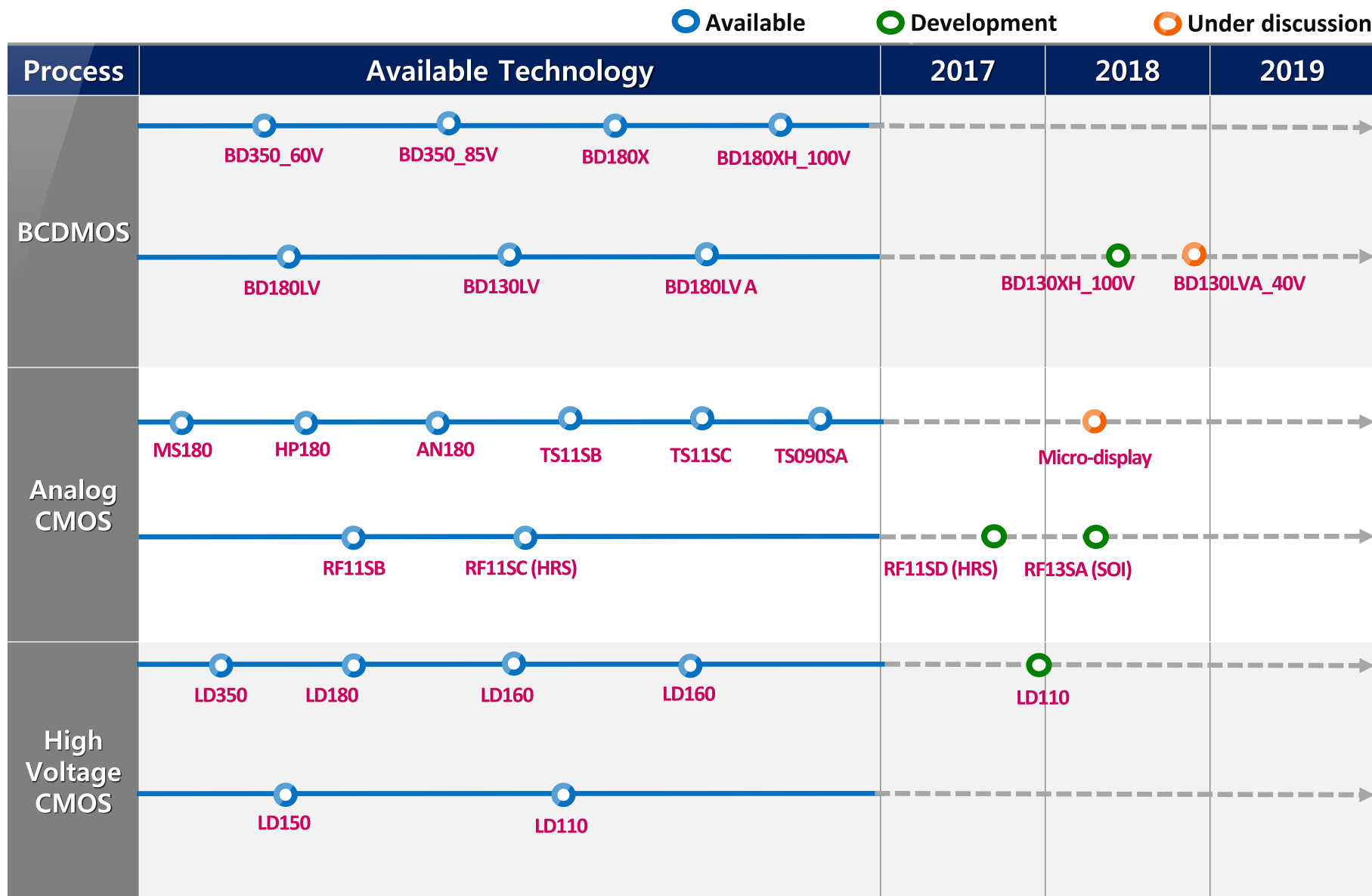
- DB HiTek support customers with valuable benefits



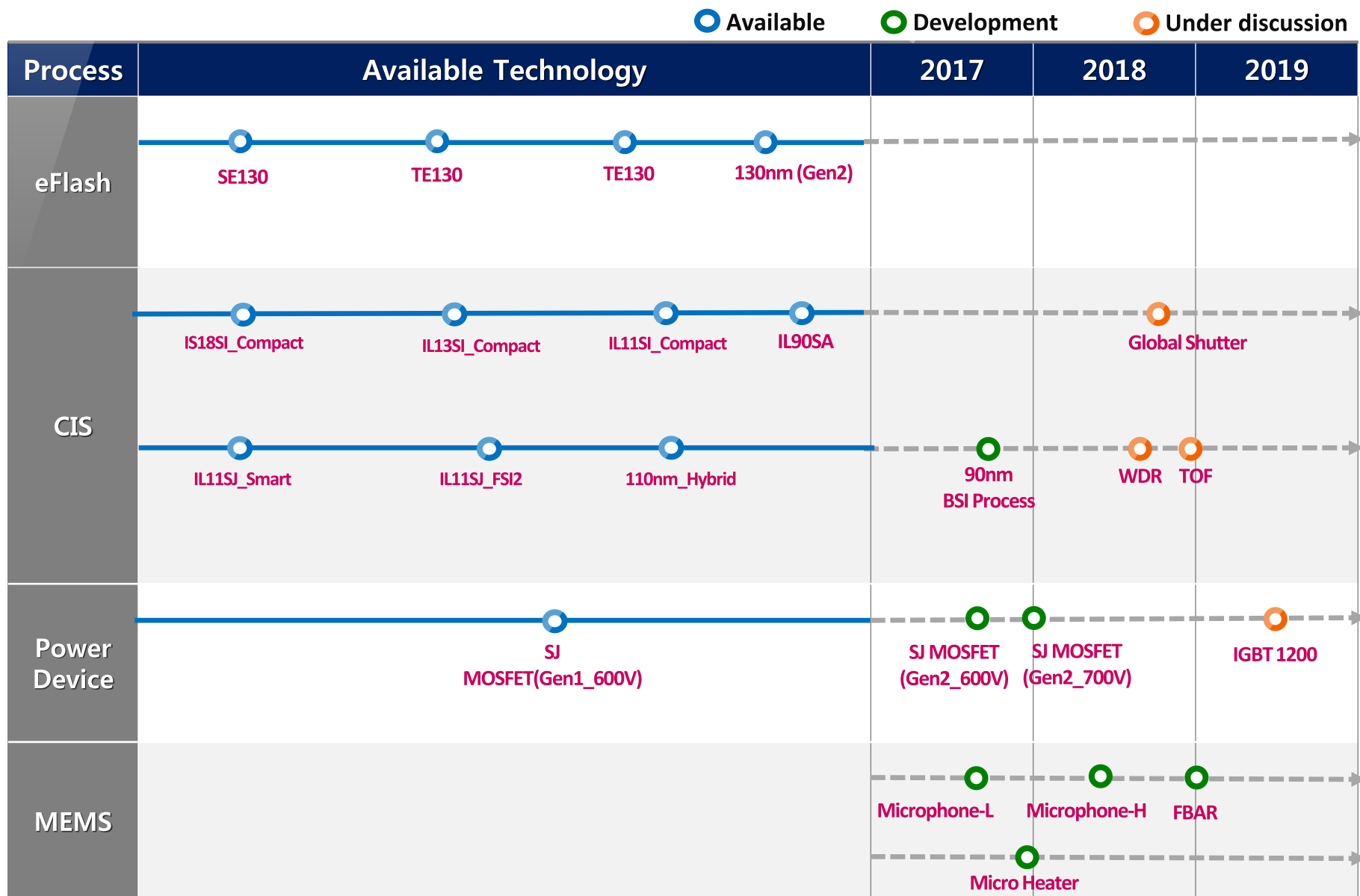
Key Process Portfolio



Technology Roadmap



Technology Roadmap



Design Environment

Design Infra

- SPICE Modeling
- PDK/iPDK
- ESD solution
- IO/STD cell Library
- Memory Compiler

Reduced
R&D
Lead Time

Application Specific IP

- Non Volatile Memory (OTP, MTP)

Reference Design Flow

- Analog/ Mixed Signal Design
- Digital Design
- EDA Solution

Partner Companies



ememory



SYNOPSYS

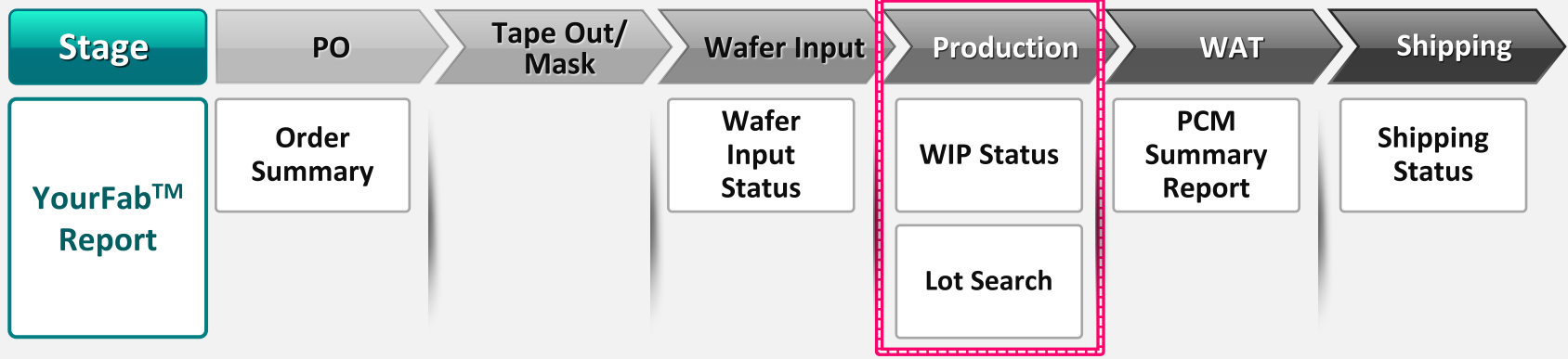
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YourFab™ Service Flow



Order To Shipping Service Flow




ShuttleChip™ Service (2017)

 Tape-out start date

Process	Tech	Fab	2017											
			1Q			2Q			3Q			4Q		
			Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
BCD (BD180LV)	0.15um	FAB1							19				08	
Analog / BCD / Mixed-Signal (AN180 & BD180 & HP180 & MS180)	0.18um		18	22	29	26	31	28	26	30	27	25	29	27
Mixed-Signal	0.11um	FAB2	18			26			26			25		
Analog / BCD (BD130)	0.13um			15		19		21		23		18		20
e-Flash	0.13um						17						15	
Mixed-Signal	0.15 ~ 0.18um				08			07			06			06
HVCMOS	0.11um					19				23				
CIS	0.11um							21				18		

- * 1. The shuttle schedule might be changed or canceled if the minimum number of paid seat has not been filled.
- * 2. Schedule for some ShuttleChip may change due to un-foreseen circumstances, so please contact your account manager for updated schedule.
- * 3. DB check will be cleared within 7 days before tape-out.

ShuttleChip™ Service (2018)

 Tape-out start date

Process	Tech	Fab	2018											
			1Q			2Q			3Q			4Q		
			Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
BCD (BEOL 0.15um, BD180LVA)	0.15um	FAB1	24			11			11		12		14	
Analog / BCD/ Mixed-Signal (AN180 & BD180 & HP180 & MS180)	0.18um		31	28	28	25	23	27	25	29	19	24	28	26
Mixed-Signal/ RF HRS	0.11um	FAB2	17			25			25			24		
CIS	0.11um							27				31		
Analog /BCD (BD130)	0.13um			21			16			22			21	
Mixed-Signal	0.15 ~ 0.18um				07			20			05			05

* 1. The shuttle schedule might be changed or canceled if the minimum number of paid seat has not been filled.

* 2. Schedule for some ShuttleChip may change due to un-foreseen circumstances,
so please contact your account manager for updated schedule.

* 3. DB check will be cleared within 7 days before tape-out.



THANK YOU

